

UNIVERSITY OF COPENHAGEN

CENTER OF QUANTUM DEVICES

BACHELOR THESIS

Fabrication of Bottom Gate Based
Semiconductor-Superconductor
Nanowire Devices

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Abstract

This thesis presents the work done on fabricating bottom gate based nanowire devices to measure Majorana bound states. It gives an introduction to realizing the Majorana bound state in 1 dimension followed by a describtion of fabricating bottomgate devices. Some of the difficulties using bottom gates will be presented as well as the development in overcoming them.

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Chapter 1

Motivation

In 1937, Ettore Majorana predicted the existence of a special particle known as the Majorana Fermion. This particle has some exiting properties which is the reason for the great experimental interest in finding evidence of its existence. Recent studies are searching for the condensed matter equivalent as zero-bias bound states in the superconducting gap. The condensed matter equivalent to Majorana Fermions are non-Abelian anyons meaning that their exchange properties are non trivial operations which make them a candidate for quantum computation [3].

Some systems have been theoretically predicted to host Majorana Fermions [7], but lately the focus has turned towards nanowires in close proximity to a s-wave superconductor [1] [2]. This system is thought to be an experimentally advantageous environment to measure the Majorana bound state because of its properties. A strong spin-orbit interaction, combined with a large g-factor and proximity induced superconductivity should give rise to a delocalized fermionic state protected from decoherence[3].

Mourik et al have measured signatures of Majorana Fermions in a device using InSb-nanowires with normal and superconducting contacts[1]. Using bottom gates covered in a thin Si_3N_4 dielectric they are able to create tunneling barriers and controlling the chemical potential of the wire. While their measurements are inconclusive their device setup is of great interest.

Anindya Das et al have measured a zero-bias peak in an Al-InAs nanowire but they have been unable to completely determine whether the zero-bias peak originates from The Majorana Fermions or it is caused by other effects[2].

During measurements some sidegates may prove to be ineffective and it has been questioned if a setup with bottom gates is more efficient in measurements as well as easier to fabricate. This thesis will give insight to the fabrication development of bottom gate based nanowire devices.

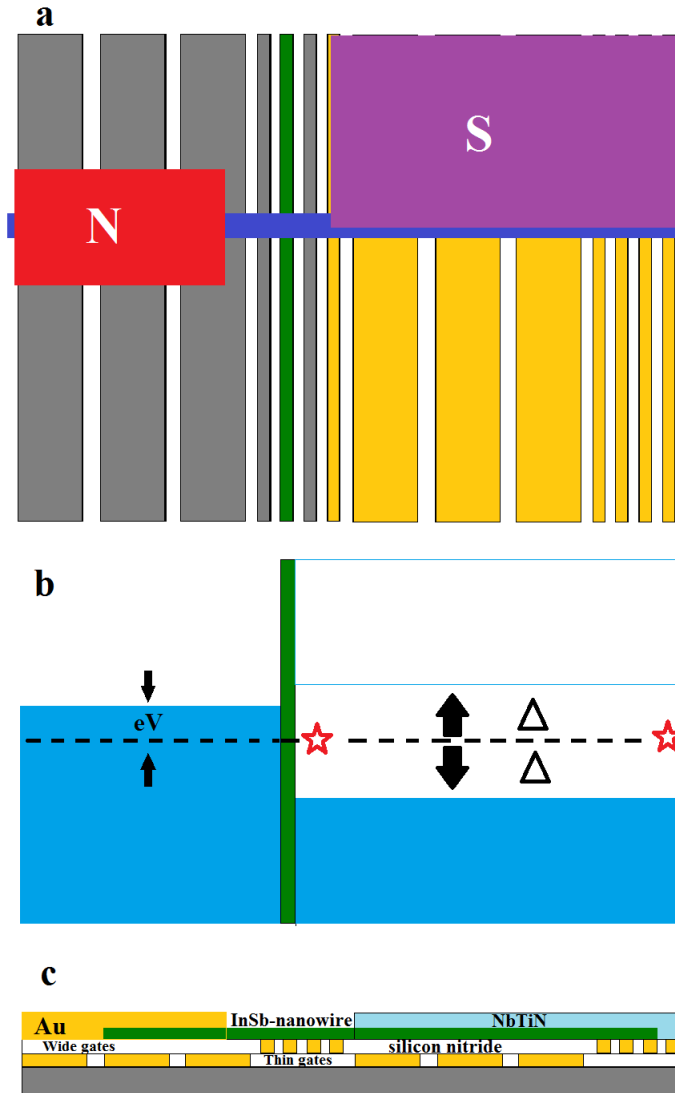


Figure 1.1: Illustration of the device made by Mourik et al. (a) Their device is made with normal (N) and superconducting (S) contacts. The S-contact covers half the wire to avoid absolute screening of the bottom gates. The bottom gates that have different numbers can be individually tuned to change the chemical potential of the wire. (b) Illustration of energy states. The green gate is used to create a tunneling barrier that separates the normal part of the wire from the superconducting part. An voltage is applied between N and S that is used to measure the density of states. The red stars indicate the location of the Majorana Fermions in the wire. (c) Schematic of the device made by Mourik et al seen from the side. The wide gates are made first and covered in 40 nm of the dielectric material Si_3N_4 . The thinner gates are made in a separate fabrication step to reduce proximity exposure. These thin gates are then covered 40 nm of Si_3N_4 . The InSb-nanowire is contacted to a Ti/Au-contact and the superconducting is made of NbTiN but only covers one side of the nanowire.

Chapter 2

Theory

The purpose of this chapter is to give a short theoretical description of the Majorana Fermion in solids as well as material requirements for realizing the Majorana Fermion.

2.1 Superconductivity

Some materials have the property of being superconducting below a critical temperature, T_c (a critical current, I_c , and a critical field, B_c). From a material with normal electrical resistivity the transition to superconductivity occurs when the material is cooled below T_c and lattice vibrations become slow. An electron will be screened by nearby lattice ions, creating a higher positive charge density around the electron, and thereby interacting with other electrons because of the deformed lattice. These electrons are now bound in pairs (Cooper pairs) with spin 1 or 0 giving it properties of a boson. An energy gap of 2Δ is opened at the Fermi level and unbound electrons among other particles are separated from the Cooper pairs by Δ in energy. Cooper pairs cannot be scattered which is the cause of zero resistance in superconductors. To split the Cooper pair an energy of more than 2Δ is required.

2.2 Majorana Fermions

All elementary particles have some attributes they can be characterized by. This could be electrical charge and spin. The spin of the particle determines whether it is a boson (integer spin) or fermion (half integer spin) giving them different properties. Each elementary particle has an antiparticle that has the same spin and mass but opposite charge of the particle. One of the most common examples being the electron and the positron. Ettore Majorana predicted the existence of what is called the Majorana Fermion, a charge neutral, spin half particle that is its own antiparticle. They may appear as elementary

particles but recently most studies try to find evidence of its existence as a quasiparticle in a superconductor. Majorana Fermions in condensed matter physics is a quasiparticle with half spin. This quasiparticle is a superposition of half an electron and half a hole (the electrons antiparticle in solid state systems). One of the reasons for the massive interest is the special exchange statistic. They are non-Abelian anyons, which mean their exchange operators are non-trivial and in general do not commute. Usually the exchange operation is a trivial case of multiplying the wavefunction with $+1$ for bosons, -1 for fermions, and a phase ϕ for Abelian anyons.

2.3 Second Quantization

Second quantization language is made for describing and analyzing many-body problems in quantum mechanics. It will be introduced to describe the $1D$ tight-binding chain and where the Majorana Fermion emerges. For fermions the creation operator is denoted as c_σ^\dagger and c_σ for the annihilation operator with spin projection σ . Other quantum numbers are not relevant here and are neglected. These creation and annihilation operators can be written in terms of a Majorana operator.

$$c_i = \frac{\gamma_{i,1} + i\gamma_{i,2}}{2} \quad (2.1)$$

$$c_i^\dagger = \frac{\gamma_{i,1} - i\gamma_{i,2}}{2} \quad (2.2)$$

Here c_i^\dagger is the creation operator on site i . Since one electron is a superposition of two Majorana Fermions then one fermionic operator is a superposition of two majorana operators in the same site.

Isolating the Majorana operators in these equations gives:

$$\gamma_{i,1} = c_i^\dagger + c_i \quad (2.3)$$

$$\gamma_{i,2} = i(c_i^\dagger - c_i) \quad (2.4)$$

For these operators it holds that they are hermitian $\gamma_{i,j} = \gamma_{i,g}^\dagger$ and thus truly they are

creation operators for the Majorana fermion.

2.4 1D tight binding chain

The tight binding chain is based on neutral atoms which are brought together when forming a crystal. In the beginning the wave functions of the electrons are only present around each atom, but when they are brought closer together their wave functions overlap. The electrons can lower their energy by being halfway between the two atoms. This allows electrons to be exchanged between the nuclei. Using second quantization language it will be shown how localized Majorana fermions exist in nanowires.

The Hamiltonian for the tight binding chain with possibility for superconductivity where t and Δ are taken to be real.

$$H = -\mu \sum_{i=1}^N n_i - \sum_{i=1}^{N-1} [t * (c_i^\dagger c_{i+1} + c_i c_{i+1}^\dagger) + \Delta c_i c_{i+1} + \Delta c_{i+1}^\dagger c_i^\dagger] \quad (2.5)$$

μ is the chemical potential, $n = c_i^\dagger c_i$ is the number operator along with the creation (c_i^\dagger) and annihilation (c_i) operators, Δ is the superconducting gap, and t is known as the hopping term.

The first term is the kinetic and potential energy of a single electron and nucleus, summed by the number of nuclei and electrons in the system. This is the term from the N isolated atoms that are used to form the chain. Next is the hopping term that allows electrons to move between neighboring sites. $t = 0$ is equivalent to a large space between the nuclei where no part of the electron wavefunction overlap and Δ is the size of the superconducting gap. The spinlabel is not considered since the electrons with the same spin pair up creating a spinless environment.

Inserting Majorana operators in the equation yields:

$$H = \frac{-\mu}{2} \sum_{i=1}^N [1 + i\gamma_{i,1}\gamma_{i,2}] - \frac{i}{4} \sum_{i=1}^{N-1} [(\Delta + t)\gamma_{i,2}\gamma_{i+1,1} + (\Delta - t)\gamma_{i,1}\gamma_{i+1,2}] \quad (2.6)$$

The Hamiltonian will be considered in two limiting cases. The first case is where $\mu < 0$ and $t = \Delta = 0$. It is a topological trivial phase where the second som of the equation (2.6) vanishes coupling Majorana operators on the same site i , figure 2.1 a. In the case that $\mu = 0$ and $t = \Delta > 0$ the Hamiltonian becomes.

$$H = -it \sum_{i=1}^{N-1} \gamma_{i,2} \gamma_{i+1,1} \quad (2.7)$$

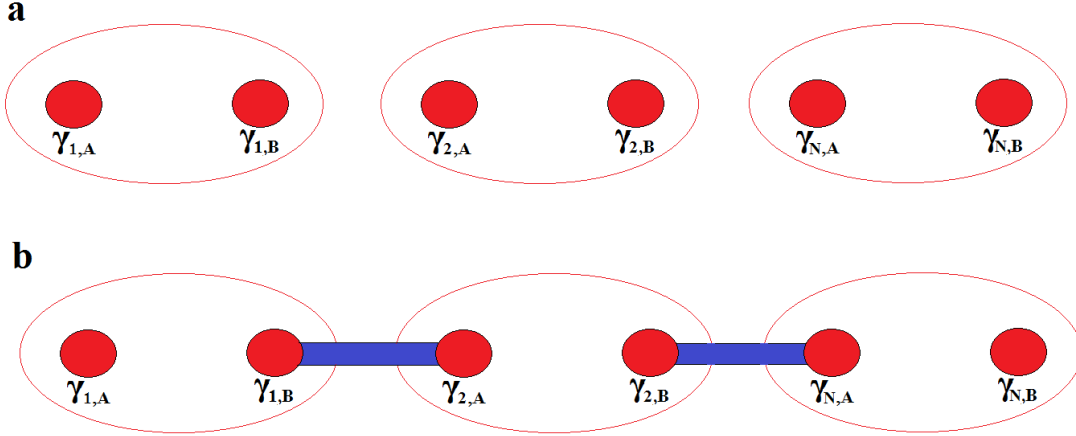


Figure 2.1: Illustration of a 1 dimensional chain where the fermionic operators are split into two Majorana operators.

(a) Situation where $\mu \neq 0$ and $\Delta = t = 0$ results in the trivial coupling of Majorana operators.
(b) Situation where $\mu = 0$ and $\Delta = t > 0$ which results in coupling of Majorana operators on neighbouring sites leaving two Majorana operators $\gamma_{N,2}$ and $\gamma_{1,1}$ unpaired.

In equation (2.6) a single site hosted two Majorana operators. Now the Majorana operators are paired to a neighboring site leaving $\gamma_{i,1}$ and $\gamma_{N,2}$ at the ends of the wire out of the equation. Combining these Majorana operators give a single fermionic operator that is missing from the Hamiltonian and the state appears at zero energy, figure 2.1 b.

2.5 P-wave Superconductivity

Superconductivity in its most common form is called s-wave superconductivity. After the phase transition from normal material to superconductor, the electrons pair up so they have opposite k-vectors and opposite spin projections. This way the cooper pair effectively has 0 spin. For a material to host Majorana Fermions a key property is a spinless environment. The required conditions for hosting a Majorana Fermion will be explained starting from the energy dispersion of a 1 dimensional material. The energy dispersion has the form $\frac{\hbar^2 k^2}{2m}$ and is spin degenerate. The spin band split in the presence of a spin-orbit interaction as the energy is now both spin and momentum dependent, figure 2.2 a. The strength of the spin-orbit coupling determines the size of the band splitting. In figure 2.2 b, an external magnetic field is applied normal to the magnetic field induced

by the spin-orbit.

This results in a gap opened at $k = 0$ of magnitude

$$2E_z = g\mu_B B \quad (2.8)$$

where g is the Landé g -factor, μ_B is the Bohr magnetron and B is the size of the external magnetic field. A spinless environment is created in the gap as the spin projection are aligned with the Zeeman field. Bringing a superconductor in close proximity to the nanowire opens a superconducting gap at the chemical potential. Depending on the relation between the Zeeman gap and the superconducting gap energy the nanowire can be either normal, figure 2.2 c, or topological, figure 2.2 d, superconducting.

The system is described by equation (2.9).

$$C = \Delta^2 + \mu^2 - E_z^2 \quad (2.9)$$

When $C > 0$ the system is in the normal superconducting phase as electrons with opposite spins form Cooper pairs. For $C < 0$ the system is in the topological superconducting phase where electrons with the same spin projection form Cooper pairs. It is important to use materials with a large g -factor as the Zeeman energy must exceed Δ before the B reached B_c . In figure 2.2 e, the slope is illustrated by the yellow lines and is proportional to the g -factor.

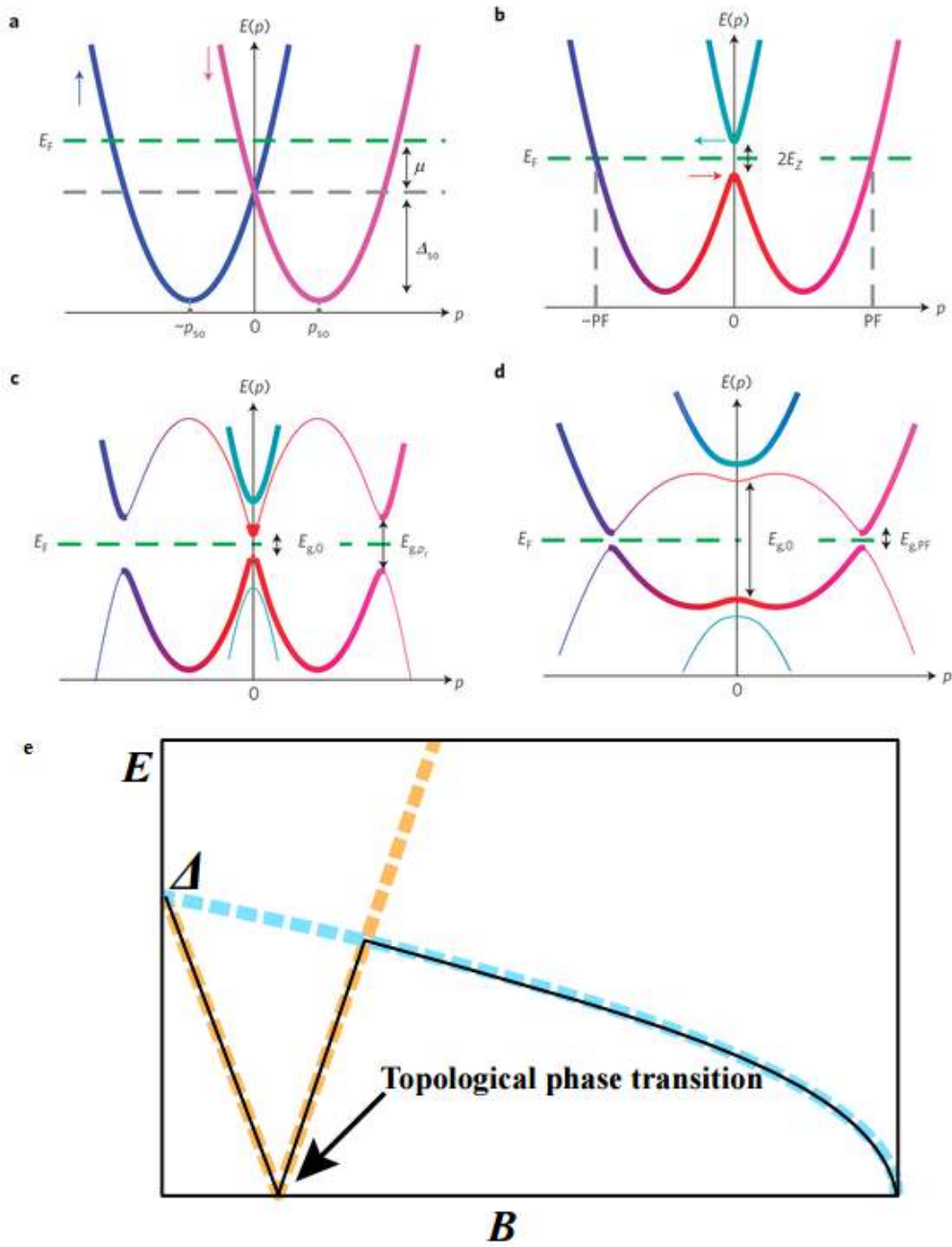


Figure 2.2: 1 D energy dispersion of a nanowire in proximity to a superconductor [2]. Heavy lines represent electron bands and light lines represent the hole equivalent. Spin directions are denoted as different colors. Blue and mangenta for opposite directions in the effective spin-orbit field while red and cyan denote opposite spin directions perpendicular to the spin-orbit field (parallel (and antiparallel) to the extern zeeman field). Color mixtures represent relative mixed spin directions. (a) The original spin degenerate energy dispersion is split due to spin-orbit coupling with spin-orbit energy Δ_{so} and chemical potential μ . (b) An external magnetic field is applied to the system causing a zeeman gap E_z at $p = 0$. (c) A superconductor in close proximity opens a superconducting gap at μ . (d) Same situation as c but with a larger zeeman gap E_z . (e) Energy at $p = 0$ (yellow) and $p = p_F$ (blue) as function of field where black line shows the overall energy gap.

Chapter 3

Fabrication and Measurement

To be able to measure a zero bias peak the system must meet certain characteristics. The first is a (large) superconducting gap that is not destroyed by a wide range tuning of the Zeeman field, a strong spin-orbit effect, the ability to tune the chemical potential. Turning the system into a p-wave superconductor and doing tunneling spectroscopy measurements should reveal a zero bias conductance peak. The purpose of this chapter is to explain the fabrication process of this kind of mesoscopic electrical devices. It gives insight to the machines used, the complications, and changes to the fabrication method.

3.1 Bottom gates versus Side gates

Most devices made prior to this project were made with side gates. One of the reasons side gates were chosen was due to the randomness of nanowire deposition within the target area (neither position or angle could be controlled). The side gate design could be made after wire deposition and adjusted to fit any position or angle. To be able to tune the chemical potential of the nanowire the gates were designed at a distance of $50nm$ to the wire along with a similar distance to other gates. Due to small misalignment and an exposure proximity effect (regions of resist close to the e-beam exposed area are destroyed as well), at best the gates could be shifted to one side resulting in a difference in gate efficiency. At worst the gates short-circuited with each other or the nanowire. As designing and fabricating side gates and contacts is one of the last steps this would result in ruined devices and a lot of wasted time. This is one of the problems bottom gates could resolve. As the name suggests the gates are fabricated before the nanowires are deposited. As the bottom gates are prefabricated the distance between the gates should be constant. To avoid shorting the gates and the nanowire, a layer of dielectric material is placed between the nanowire and the bottom gates. This way the distance from the bottom gates to the nanowire is equal to the thickness of the dielectric material. One

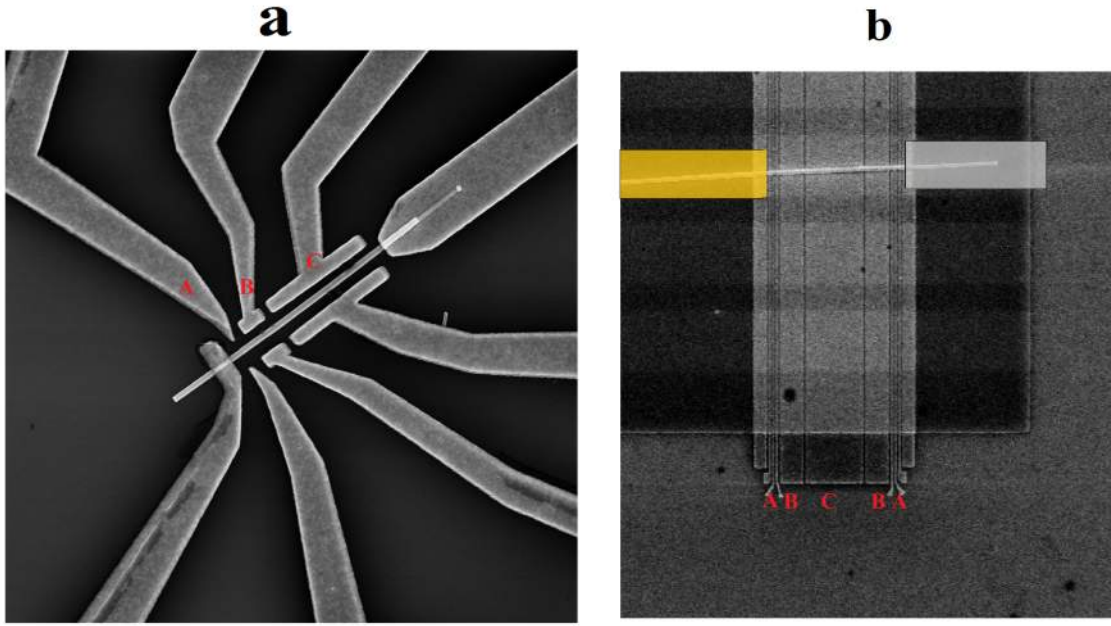


Figure 3.1: Picture of two gate designs.

(a) A device with side- and plunger gates distributed along the wire with Au and superconducting contacts at the ends.

(b) Picture of a the bottom gate devices with contacts drawn on the picture. The letters A, B, and C show which bottom gates corresponds to the side gates. The bottom gate device consists of 2 nanowires that are connected through a superconducting contact. Au and superconducting contacts were later fabricated on each end. The layer of HfO_2 has changing brightness due to E-beam exposure when making wire-windows. The wire has landed in one if these windows and is almost perpendicular to the bottom gates

problem to solve is how to deposit and align the nanowires perpendicular to the gates.

3.2 Devices

The design is a normal material, nanowire, superconductor (N-NW-S) setup with bottom gates, see figure 3.2. The first step is to make bottom gates that are not shorted or broken. These gates are later connected to meanders and used to tune the chemical potential of the nanowire in different segments thus making tunneling barriers and increase or decrease the electron density in the wire. A thin layer of the dielectric Hafniumoxide (HfO_2) is located between the bottom gates and the nanowire, that will prevent any current leaking from the gates to the nanowire. When a gate voltage is applied, it will induce an electric field in the HfO_2 affecting the chemical potential of the wire. By creating a tunneling barrier and applying an external bias voltage (DC voltage with a small, high frequency sinusoidal modulation) between the normal and superconducting contact the differential conductance dI/dV can be measured at voltage V as illustrated in figure 1.1b.

This differential conductance is proportional to the density of states in the nanowire. A conductance peak at zero bias would indicate a Majorana bound state if it is stable at various magnetic fields but vanishes when the Zeeman field is parallel to the effective spin-orbit field.

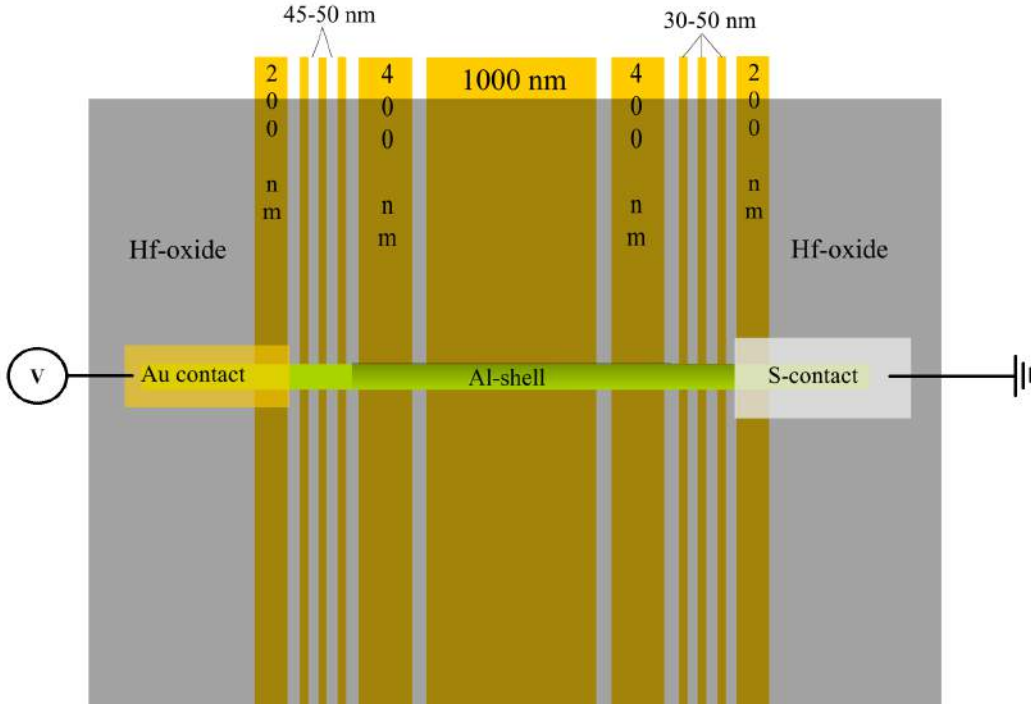


Figure 3.2: Illustration of an ideal bottom gate device. Two different designs are described by two options of width indicated. Bottom gates are supposed to tune the chemical potential in the InAs-nanowire and create tunneling barriers. A 20nm layer of HfO_2 is fabricated on top of the bottom gates. The wire has one Au contact and one contact of a superconducting material. The aluminum shell is etched at the end of the gold contact to make it easier to make potential barriers in the wire.

3.3 Fabrication Chips

The devices were fabricated on silicon chips, that were made from a silicon wafer that was oxidized to form an insulating layer of SiO_2 . On one side the SiO_2 was removed and Ti plus Au deposited. The chips are $5\text{mm} \times 5\text{mm}$ and the chip area is divided into 4 quadrants. These quadrants all have 40 bonding pads and meanders with equal length therefore equal resistance. The bonding pads are used to connect the devices fabricated in the center of each quadrant to measuring equipment through the meanders. Four alignment marks are placed in each quadrant to align the chip when using the EBL. The center of the quadrants are composed of 100 small squares that can be individually identified by the marks in each corner.

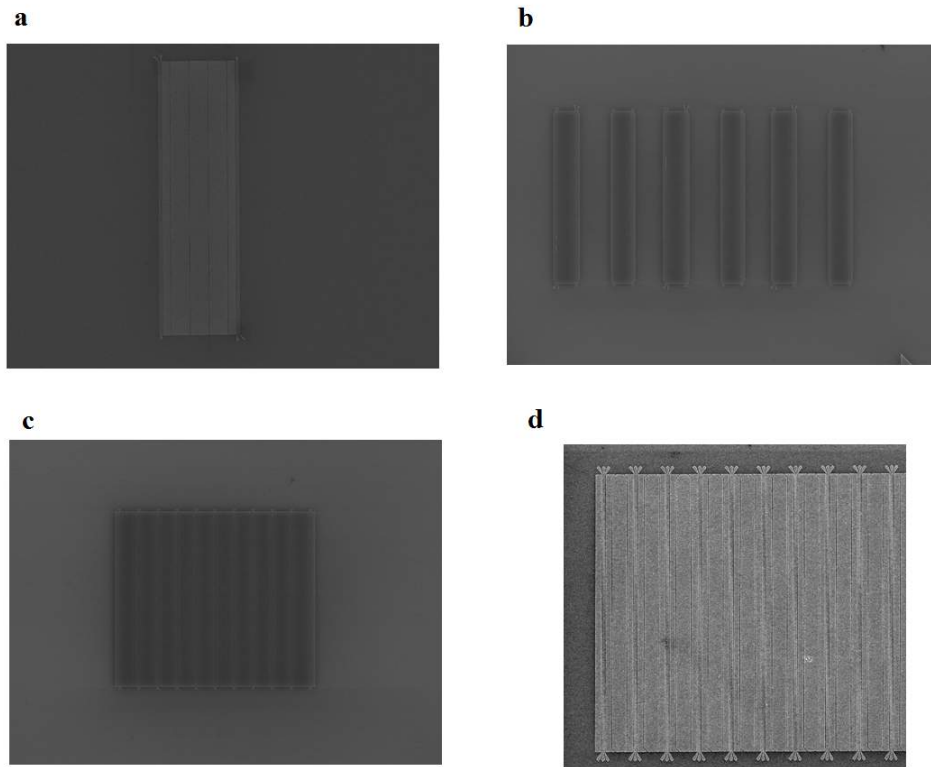


Figure 3.3: A picture series illustrating the design development of bottom gates.

(a) Picture of the earliest bottom gate design. 100 of these designs were on the target area on the chip.

(b) Improved design where 600 bottom gate designs were made on the chip to increase the chance of a wire being deposited the right way.

(c) Array of bottom gate designs leaving no space in between gate designs as in (b).

(d) Almost same design as (c) but with increased size of the ends of the thin gates to make it easier to connect to meanders.

3.4 Bottom gates

The bottom gates are the first fabrication step but there was no recipe telling which resist to use or the dose (μ/cm^2) for the electron beam lithography (EBL). A dose test was made with A2 to be able to make fine features without resist tilting due to the thickness of the resist. The dose test was done for two types of designs. One where the gates were designed as rectangles which are converted to an area of dots that are exposed by the EBL. Another where the gates were single pixel lines. Similar bottom gate designs were made with increasing dose. After development, metal evaporation, and lift-off the results could be compared. Some dose values resulted in the resist being underexposed where unexposed resist would stick to the surface after development so the evaporated metal would never reach the surface resulting in broken and useless gates. Other dose values were too high leaving no resist to separate the gates shorting them all. A dose value with

repeated good results were chosen.

In the beginning the bottom gate design was single designs made across the chip 3.3 a. Later it became difficult to deposit wires that landed in a way so they could utilize the bottom gates. Later several bottom gates were made side by side to increase the chance of a wire landing on top see figure 3.3 b. Even so the design ended up being an continuous array covering large areas of the quadrants see figure 3.3 c.

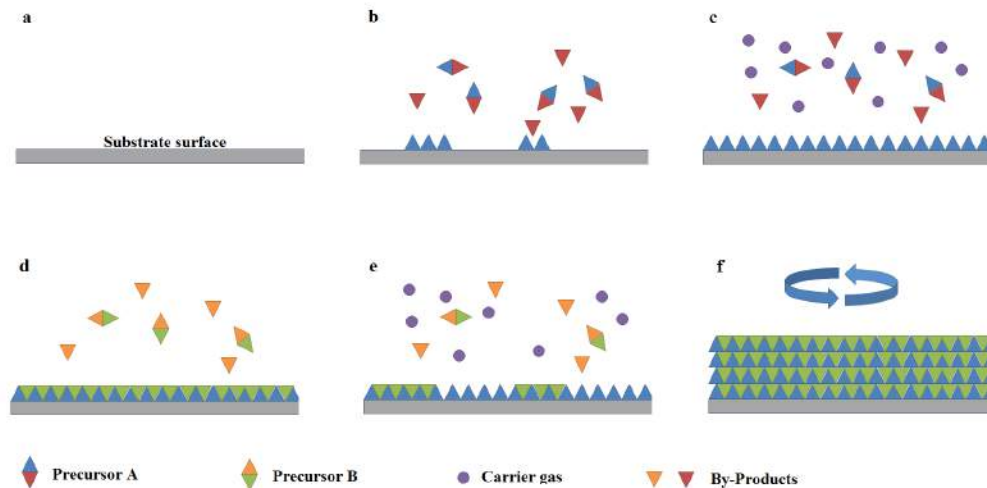


Figure 3.4: ALD illustration. (a) The surface of the substrate. (b) The first precursor A is pulsed into the chamber reacting with the surface substrate leaving by-products. (c) A carrier gas removes any reaction by-products and remaining precursor. (d) Precursor B is pulsed into the chamber reacting with the surface. (e) Carrier gas removes any reaction by-products and remaining precursor. (f) This cycle is repeated until the final thickness of the material is achieved.

3.5 ALD Hafniumoxide

After fabricating the bottom gates on the silicon chip it is time to apply the layer separating the bottom gates and nanowire. This process is called atomic layer deposition (ALD) and is capable of producing very precise nanometer thick films. Other advantages are the capability of depositing to almost any structure and a limiting characteristic which ensures only one layer of the deposited material reacts with the surface and therefore a uniform thickness. The ALD process will deposit the material to any surface which is undesirable when several fabrication steps are yet to be completed. Before depositing Hafniumoxide (HfO_2), the chip is coated in resist, and an ALD-window is made in the resist above of the bottom gates this ensures the HfO_2 only reacts with the chip surface in the opened window. The chip is placed in a vacuum chamber for the duration of the pro-

cess. The ALD process is a sequence of pulses. At first a precursor (chemical containing Hf) is pumped into the chamber in gaseous form and is given time to fully react with the surface of the chip see figure 3.4 b. Meanwhile a carrier gas (N_2 in this case) is pumped into the chamber removing the remaining precursor and any reaction by-products, figure 3.4 c. This is followed by another precursor pulse of H_2O which is commonly used to make oxides, figure 3.4 d, and a purge of carrier gas, figure 3.4 e. During this cycle, one monolayer is left at the surface. The cycle is repeated until the desired amount of layers have been made.

3.6 Nanowires

Semiconducting indium arsenide (InAs) nanowires are essential to the search for Majorana Fermions. Due to their strong spin-orbit coupling and large g-factor they are suitable for Majorana Fermion experiments. Following nanowire growth they are coated in epitaxial aluminum shell. This could be either half shell or full shell. This way the interface between InAs and the aluminum shell has no oxide layer and therefore good electrical contact. One of the requirements for a hard gap is met by the good nanowire superconductor interface. The aluminum shell makes better contacts since it is metal on metal contact. Half shell nanowires are well suited since their chemical potential is tunable by the bottom gates.

When depositing wires to bottom gates it was ideal that the wires landed on top of the gates, aligning perpendicular to the direction of the gates. To increase the chance of this event, a layer of resist would be spun on the chip. After baking wire windows would be exposed on top of the bottom gates. These wire windows are recesses in the resist significantly larger than the wires in length and width. The wires that were deposited on to the bottom gates would now fall into the wire windows and automatically align perpendicular to the gates the intended way, figure 3.1 b.

The deposition of the wires is done with a clean room tissue that is cut into small triangles. The tip of the triangle is then gently rubbed on the growth substrate. The nanowires will then be attached to the tip of the tissue. The tip is gently moved across the area of the chip with bottom gates parallel to the direction of the wire windows. A microscope was used to check if a reasonable amount of wires had landed on the bottom gates. More wires would be deposited if only few wires were in the desired region. An E-Line scanning electron microscope (SEM) was used to locate the nanowires on the chip. Images of each quadrant were taken and from these the wires with a suitable position and alignment relative to the bottom gates were chosen. Position coordinates were logged along with

the images to determine the exact location of the wires and make the device design with small misalignment.

3.7 Resist

Making devices can be a difficult task that requires precision in tenths of nanometers or less. When milling or doing metal deposition a protective coat is needed to ensure that the chip or device is left unchanged. For this task polymethyl methacrylate (PMMA) or methyl methacrylate (MMA) are commonly used. PMMA and MMA are materials suited for high resolution imaging using an electron beam, as well as protective coating. When exposed to a e-beam the polymer chains are broken down in the exposed area, creating well-defined transition between areas of exposed and unexposed PMMA. MMA consists of shorter polymer chains than PMMA and is more susceptible to the e-beam and is broken down further from the actual exposed area and could be used in combination with PMMA to create undercuts or design top gates. After exposure a developer was used to remove the exposed PMMA. A developer composition of MIBK:IPA (1:3) was used to dissolve the exposed resist before the chip was ashed. Ashing is a process where the chip is exposed to oxygen plasma that react with the residual that is pumped out due to a vacuum leaving a clean surface.

It is the current fabrication step that determines what kind of resist that is spun on the chip. Exposed PMMA on top of MMA would result in a undercut while the reverse order would be suitable for making top gates. PMMA and MMA exist in various resist dilutions that give different film thickness when spun at a certain rate. The film thickness should be larger than the thickness of the evaporated metal, without causing the resist to tilt. The lift-off was done with NMP (Dioxylane and Acetone) that dissolve the resist after metal deposition. This process removes resist along with the deposited metal attached to it.

3.8 Metal Deposition

The AJA machine was used for metal evaporation and milling in a single chamber with a high vacuum. This way the sample is not exposed to oxygen during milling or repeated metal evaporations, leaving no oxide layer. For metal evaporation the machine generates a powerful electron beam and aims it at the target metal crucible at the bottom of the machine to vaporize it in the vacuum. Due to the high vacuum the mean free path of the evaporated particles are longer than the distance from the crucible to the sample. This

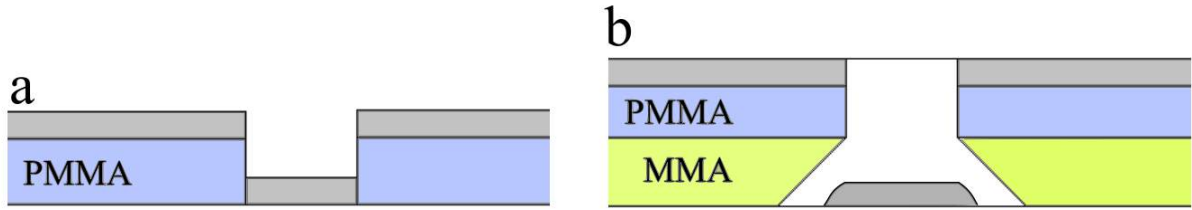


Figure 3.5: Illustration of exposed resist with evaporated material.

(a) Illustration of exposed PMMA after metal evaporation. The metal on top of the resist will be removed during lift-off but the metal on chip will stay.

(b) Illustration of exposed MMA and PMMA. This will create an undercut and the material on the chip will have round edges.

ensures a controlled process where the thickness of the evaporated material is accounted for by the machine. There are several materials available but the most commonly used were Ti, Au and Al.

The nanowires are made of InAs with Al shell which will develop a thin oxide layer when exposed to air. This InAs-oxide or Al-oxide needs to be removed by milling the sample before evaporation to make a clean contact. Ion milling is a technique where (argon)ions are accelerated from the ion-source into the chip thereby removing the outer layers of atoms. The milling rate varies from material to material and it is important not to mill longer than necessary as it can contaminate the sample. Al-oxide was milled before making a superconducting contact while InAs-oxide was milled before making gold contacts.

3.9 Etching

Before gold contacts can be fabricated it is important to remove the aluminum shell from the nanowire. Otherwise the measured current would go through the aluminum shell and not the InAs-nanowire. The current must go through the wire because of its properties (large g-factor, strong spin-orbit) which are not present in the aluminum shell. Only a part of the shell is etched as it is still needed to induce proximitized superconductivity in the wire. To protect the wires from being fully etched the chip is coated in PMMA. A small etching-window is opened in the end of the wire opposite to the superconducting contact. The etching-window extends across the three narrow gates so they are able to tune the chemical potential of the wire in a more efficient way.

The etching is done with a chemical called Aluminum Etchant D in a hot bath where the etching rate is known. First of all the chip is lowered in Milli-Q water to avoid any

air trapped in the etching-windows. Then is it etched for 10 seconds and then quickly transferred and rinsed in Milli-Q water and IPA to stop the etching process. During this time the etchant will not only etch the exposed aluminum shell but etch 50nm further under the resist therefore the etching-window is shifted 50nm to one side to compensate, figure 3.6.

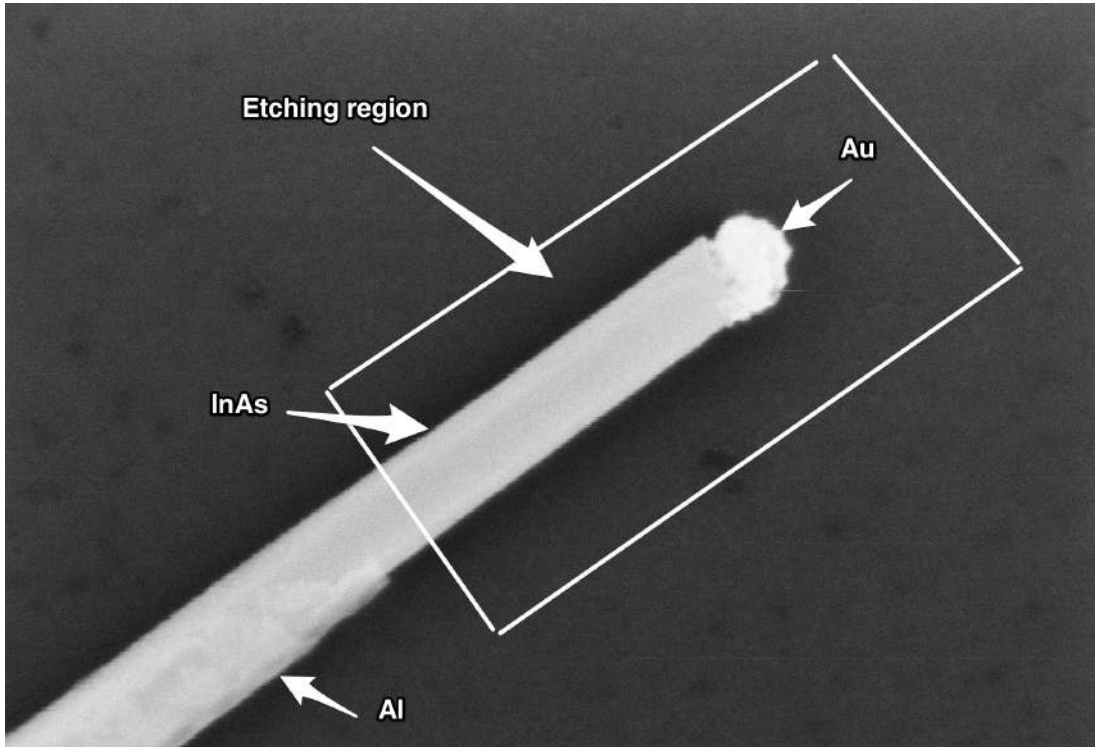


Figure 3.6: SEM picture of the end of an InAs-nanowire after aluminum etching. The aluminum shell is completely removed in the etching region equivalent to the etching window sketched in the picture. The distance from the etching region to the aluminum shell is caused by the etchant. The Au particle used in the nanowire growth can be seen as well.

3.10 Results

One of the objects of this thesis was to do low-temperature measurements on nanowire devices. Though the fabrication might seem straightforward but when fabricating mesoscopic electric devices errors on the scale of tenths of nanometers could result in devices that do not work as intended. On this scale it is not easy to realize an error has been made before the devices have been tested. Some of the mistakes can be attributed to bad choices during but other mistakes could be hard to avoid. Each fabrication step increases the risk of defects in the devices and using bottom gates introduces a few more fabrication steps even though these steps do not directly affect the nanowires. There were some fabrication steps that involved a higher risk than others. Fabricating the bottom

gates, etching, and milling before material deposition. Due to the small width between the small gates, they would sometimes have defects because of the e-beam lithography or development. A solution could be to try a new CSAR resist and/or development. This resist has a sub $10nm$ resolution and a higher sensitivity to the e-beam than PMMA but one of the benefits is a higher contrast. Trying cold development might reduce erosion of unexposed areas. This might reduce the defects on the bottom gates and result in a higher yield in future fabrication. Separate tests (dose test for the new resist and development tests) would have to be made to see which combination of resist and development that yields the best results. With the current yield of the bottom gates it would seem like an improvement to side gates from a fabrication point of view due to the uniform design, and that this fabrication step has no risk of shorting to the nanowire.

Chapter 4

Conclusion

The purpose of this thesis was to introduce the basic theory of the Majorana Fermion, and give some insight to the fabrication method of creating bottom gate based semiconductor-superconductor nanowire devices, that are able to measure and manipulate Majorana bound states. Experiments by Mourik et al have shown signatures of the Majorana Fermions and this project set out to use a similar design with bottom gates to replace side gates.

Even though the fabricated devices showed promising results on SEM images and had no shorts, no measurements were done on any devices due to fabrication errors along the way. Some errors occurred during the fabrication of the bottom gates and some during etching and milling. Some tests with resist and development need to be done to increase the fabrication yield but it seems advantageous to change to bottom gates from a fabrication perspective point of view.

The most important work still needs to be done. Fabricating a functional device that can be measured will give some knowledge of the benefits of bottom gates as well as search for Majorana Fermions. Given the prior knowledge and measurements with side gates, pros and cons of bottom gates and side gates can be evaluated the choice of future gate design could be made.

The search for Majorana Fermions has attracted a lot of attention for many years. Measurements show signatures of Majorana bound states and the question might not be if but when the manipulation of the Majorana bound state leads to braiding and quantum computation. Hopefully this thesis has made a small contribution to this research.

.1 Appendix A

.2 Recipes

In this appendix the recipes for making a device with bottomgates are given here. For further details see logbook.

.2.1 Bottomgates

Resist

- Remove existing resist/clean chip. Rinse in Acetone, IPA and blow dry with air gun.
- Spin A2 at 5000 rpm for 60 seconds.
- Bake at 185deg C for 5 minutes.

EBL and Development

- 240.000 Dots.
- Current 500pA.
- Write Field 600 μm .
- 1280 $\mu C/m^2$
- 60 seconds in MIBK:IPA (1:3), rinse in IPA.
- 15 seconds asher.

Metal deposition and Lift-Off

- Evaporate 5 nm Ti and 20 nm Au.
- Lift-off in NMP at 80 deg C for 30 minutes. Blow chip using pipette until gold is removed. Ultrasound for 1 minute. Rinse in Acetone and IPA.

.2.2 ALD

Resist

Chip is clean after lift-off. •Spin A4 at 5000 rpm for 60 seconds.
•Bake at 185 deg C for 5 min.

EBL and Development

- 240.000 Dots.
- Current 500pA.

- Write Field $600\mu m$.
- $1440 \mu C/m^2$ •60 seconds in MIBK:IPA (1:3), rinse in IPA.
- 15 seconds asher.

ALD

- Set reaction temperature to 90 deg C .
- Hafnium precursor pulse 0.2 seconds. Wait 100 seconds (the longer the better).
- Water precursor pulse 0.02 seconds. Wait 200 seconds.
- Repeat for 200 cycles for 20 nm HfO_2 .
- Lift-off in NMP at 80 deg C for 30 minutes. Blow chip using pipette. Ultrasound for 1 minute. Rinse in Acetone and IPA.

.2.3 Wire-Windows

- Chip is clean from lift-off. •Spin A6 at 5000 rpm for 60 seconds.
- Bake at 185deg C for 5 minutes.

EBL and Development

- 240.000 Dots.
- Current 500pA.
- Write Field $600\mu m$.
- 60 seconds in MIBK:IPA (1:3), rinse in IPA.
- 15 seconds asher.

Nanowires

- Deposit nanowires and rinse chip gently in Acetone and IPA.

.2.4 Superconducting contact

Resist

- Spin EL6 at 4000 rpm for 60 seconds to minimize risk of moving wires.
- Bake at 185 deg C for 3 min.
- Spin A4 at 5000 rpm for 60 seconds.
- Bake at 185 deg C for 3 min.

EBL and Development

- 240.000 Dots.
- Current 500pA.
- Write Field $600\mu m$.
- $1600 \mu C/m^2$
- 90 seconds in MIBK:IPA (1:3), rinse in IPA.
- 15 seconds asher.

Metal deposition

- Mill sample for 2 + 2 minutes with *1minutebreak* at 1 mTorr and 15 sccm.
- Evaporate 5 nm Ti, 100 nm AL, 2 nm Ti and 3 nm Au.
- Lift-off in Dioxylyane for 30 minutes. Rinse in Acetone and IPA.

.2.5 Etching

Resist

- Spin A6 at 5000 rpm for 60 seconds.
- Bake at 185 deg C for 5 min.

EBL and Development

- 240.000 Dots.
- Current 500pA.
- Write Field $600\mu m$.
- $1440 \mu C/m^2$
- 90 seconds in MIBK:IPA(1:3), rinse in IPA.
- 15 seconds asher.

Etching

- Chip is lowered in Milli-Q water before being etched in Aluminum Etchant for 10 seconds.
- Rinsed in two different cups Milli-Q water and then rinse with IPA.
- The resist is removed with Acetone and chip is rinsed in IPA.

.2.6 Au Contacts

Resist

- Spin EL9 at 4000 rpm for 60 seconds to minimize risk of moving wires.
- Bake at 185 deg C for 3 min.
- Spin A4 at 5000 rpm for 60 seconds.
- Bake at 185 deg C for 3 min.

EBL and Development

- 240,000 Dots.
- Current 500pA.
- Write Field $600\mu m$.
- $1600\ \mu C/m^2$ • 90 seconds in MIBK:IPA (1:3), rinse in IPA.
- 15 seconds asher.

Metal Evaporation

- Mill sample for 1 minute at 1 mTorr and 15 sccm.
- Evaporate 7 nm Ti and 95 nm Au.
- Lift-off in Dioxylane for 30 minutes. Rinse in Acetone and IPA.

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